In the Specification

Please amend the paragraph at page 14, line 11 and ending at page 15, line 12 as follows:

In the preferred embodiment the System Controller card samples the current state of the master timing counter (which is on the System Controller card) and store this value. With respect to Figure 5, when some other card requires its timer counter value to be synchronized, the System Controller can download the stored value via the bus [[504]] 505 to a local card controller 506. In theory, the local controller 506 can load the master timing counter value into a register 503 which can clock the stored value directly into the timing counter 512. Inasmuch as the timing counters all receive the same system clock signal, all of the timing counters 512 on other cards should increment in lock step thereafter. In reality however, loading the master timing counter value into the timing controller takes so much time that by the time the master timing counter value was written into the new timing counter, the real value of the master timing counter will have changed. Accordingly, the preferred methodology for updating a timing counter adds to the master timing controller value, a positive offset amount, which is loaded into the register 503 for a subsequent control signal from either the local card processor 506 or in some embodiments the System Controller. By adding a positive offset to the master timing counter and saving this value as the new value loaded into the timing controller, the resultant value can be locally clocked into the timing counter 512 by a trigger control signal 502 from the System Controller when the System Controller determines that the next value of the master timing controller will be equal the stored value in the register 503. In other words, the System Controller card increases the sampled count value by a predetermined amount in order to transform the sampled count value into a new increased value (pointing at a point in time in the future) so as to compensate for the time required to transfer the new increased value into a local register 503 from which it can be clocked under the System Controller 502 into the local timing counter 512. The increased count value should be created such that the actual loading of this increased count value into the slave timing counters (after distribution from the System Controller card to the cable interface cards) will occur exactly when the master timing counter on the System

Controller card arrives at the value which is equal to the increased value. This will keep the master timing counter and all slave timing counters in synchronization.